Electronic Version
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Description

[TWO PHASE INTERNAL VOLTAGE GENERATOR]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92118561, filed on July 8, 2003.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to an integrated circuit of an internal voltage generator. More particularly, the present invention relates to a two phase internal voltage generator providing low current consumption, which is adapted to low-power integrated circuit.

[0004] Description of Related Art

[0005] As scientific technology advances and environmental consciousness awakens, integrated circuitry proceeds towards high speed operation and low power consumption accordingly. Therefore, power saving and size reducing scheme

as well as enhanced functions are thus introduced to varieties of electronic products. It is a major object to substantially realize low power consumption for Integrated Circuits (IC), for example, low power consumption Dynamic Random Access Memory (DRAM). Undoubtedly, low power scheme is particularly significant for Personal Computer (PC) market as well as consumer electronics market.

[0006] FIG. 1 illustrates a circuit of a conventional internal voltage generator. The conventional internal voltage generator is for generating and providing steady and regulated internal voltage source, where the internal voltage source VINT is different from an external voltage source VEXT. The external voltage source varies within the range from 2.3V to 2.7 V while the internal voltage VINT is fixed at 2.1V, for example.

[0007] Referring to FIG. 1, the internal voltage generator 10 comprises a comparator 12, an NMOS power transistor 14, a resistor R1 and another resistor R2. It is known from FIG. 1 that the internal voltage generator 10 comprises a feedback loop, wherein resistors R1 and R2 serves as a voltage divider for internal voltage VINT and feeds the divided voltage back to the comparator 12. Comparison between the feedback voltage and reference voltage vREFDC per-

formed by comparator 12 hereby controls the NMOS power transistor 14 so as to obtain the internal voltage VINT.

[0008] In this conventional internal voltage generator 10, the resistors R1 and R2 are serially connected wherein the two ends of each resistor couple to the internal voltage and ground respectively, thus considerable direct current (dc current) is consumed thereby, i.e. significant dc current is consumed under active mode. Assuming the internal voltage generator applying to DRAM and the active dc current being 600μA, as the DRAM operates a self refresh, there is supposed to be 8 internal voltage generator operating simultaneously, such that an average active dc current is: 30μA=(600μA*8*100nS)/16μS, where power consumption is considerably large, which means such IC is hardly referred as a low power consumption IC that conventional internal voltage generator 10 does not qualify a low power consumption IC.

SUMMARY OF INVENTION

[0009] The invention provides a two phase internal voltage generator and a generating method to improve major power consumption problem in conventional internal voltage generator as much as to conformp6p6 to low-power con-

sumption IC.

[0010] Therefore, the invention provides a two phase internal voltage generator at least comprising a first phase internal voltage generator and a second phase internal voltage generator, wherein the second phase voltage generator consumes lower power than the first internal voltage generator. When an external voltage is received, the first internal voltage generator promptly generates a first internal voltage, yet the first-phase internal voltage generator cuts off the power provided therein when a second voltage power that is provided by the second internal voltage generator manages to be steady.

[0011] The two phase internal voltage generator as embodied and broadly described according to one preferred embodiment in the present invention herein, the second-phase internal voltage generator comprises a voltage pump generator, a input gate voltage generator, and a power output circuit. The voltage pump generator pumps up an external voltage in order to provide a pumped voltage according to a first control signal. The input gate voltage generator steps down and regulates the pumped voltage to an input gate voltage according to a second control signal. As to the power output circuit, it steadily provides the second

internal voltage source according to the input gate voltage, wherein the power output circuit may comprise a power transistor, e.g. a NMOS power transistor. The first phase internal voltage generator cuts off the first internal voltage source that is supplied therein according to a third control signal in one preferred embodiment of this present invention.

[0012] Regarding the foregoing two phase internal voltage generator in one preferred embodiment of this present invention, the internal operation steps are described as follows. As external voltage is firstly received, a first internal voltage source is provided promptly by the first phase internal voltage generator therein. A first control signal is generated thereby thus actuates the voltage pump generator to provide pumped voltage. A second control signal is then generated thereby to actuate the input gate voltage generator that provides input gate voltage as well as activates power output circuit to steadily provide a second internal voltage source. Ultimately a third control signal is generated so as to cut off the first internal voltage source supplied thereby the first phase internal voltage generator.

[0013] According to another aspect of this present invention, a two phase internal voltage generating method is provided

which complies to an integrated circuit that is composed of a first phase internal voltage generator and a second phase internal voltage generator. Notice that the second phase internal voltage generator consumes relatively lower power than the first internal voltage generator, wherein the two phase internal voltage generating method comprises the following steps successively. As external voltage is firstly received, a first internal voltage source is provided promptly by the first phase internal voltage generator therein. The external voltage is pumped by the second phase internal voltage generator to obtain a pumped voltage that is to be stepped down and regulated in order to obtain an input gate voltage, whereas second internal voltage source is thus provided according to the input gate voltage therein. Ultimately the forgoing first phase internal voltage generator cuts off the first internal voltage source accordingly.

[0014] In this present invention a structure of two phase internal voltage generator is introduced. The first phase internal voltage generator which is more power consuming promptly provides a steady first internal voltage source. As the second internal voltage provided by the second phase internal voltage generator is steadied, the first in-

ternal voltage generator cuts off the first internal voltage therein, so as to improve the issue over power consumption.

[0015] These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0018] FIG. 1 illustrates a circuit of a conventional internal voltage generator.

[0019] FIG. 2 illustrates a block diagram of a two phase internal voltage generator circuit according to one preferred em-

bodiment of this invention.

[0020] FIG. 3 illustrates the circuit of the first phase internal voltage generator 100 of the two phase internal voltage generator according to one preferred embodiment of this invention.

[0021] FIG. 4 illustrates the circuit of the second phase internal voltage generator 200 of the two phase internal voltage generator according to one preferred embodiment of this invention.

[0022] FIG. 5 illustrates an internal operating clock diagram for the two phase internal voltage generator according to one preferred embodiment of this invention.

DETAILED DESCRIPTION

[0023] Referring to FIG. 2, a circuit block diagram of a two phase internal voltage generator is illustrated according to one preferred embodiment of this present invention. This present invention provides a two phase internal voltage generator comprising at least a first phase internal voltage generator 100 and a second phase internal voltage generator 200, wherein the second phase internal voltage generator 200 consumes relatively lower power than the first phase internal voltage generator 100. For instance, as DRAM performs self-refresh, eight of the internal voltage

generators operate simultaneously consuming an average active current of 30μA while a first phase internal voltage generator 100 consumes an active dc current of 600μA assuming the first internal voltage generator 100 is introduced herein the DRAM. Contrarily, if a second internal voltage generator 200 is introduced to a DRAM circuit, an average active current consumption is merely 0.5μA as calculated accordingly.

[0024] One object of the first phase internal voltage generator 100 is to provide a steady first internal voltage source, which is expressed as VINT1 herein. While the power is operating, the first phase internal voltage generator 100 promptly provides a steady first internal voltage source as long as an external voltage source VEXT is detected. In this one preferred embodiment, the first phase internal voltage generator 100 cuts off the first internal voltage source according to a third control signal CHRDY3. Whereas the second internal generator 200 is introduced to provide a steady second internal voltage expressed as VINT2. One of the characteristics of this present invention is as the second internal voltage source provided by the second phase internal voltage generator 200 is regulated, the third control signal CHRDY3 actuates the first phase

internal voltage generator 100 so as to cut off the first internal voltage source therein.

[0025] Referring to FIG. 3, a circuit diagram of the first phase internal voltage generator 100 of the two phase internal voltage generator in FIG. 2 is illustrated herein. In FIG. 3, the first phase internal voltage generator 100 comprises a comparator 102, a NMOS power transistor 104, a first resistor 106, and a second resistor 108. It is noted that the first source/drain terminal of the NMOS power transistor 104 couples to an external voltage source, where an internal VINT1 is output accordingly. A first terminal of the first resistor 106 couples to a second source/drain terminal of the NMOS power transistor 104, whereas the first terminal of the second resistor 108 couples to the a second terminal of the first resistor 106 so as to provide feedback voltage. A second terminal of the second resistor 108 is grounded. The first internal voltage VINT1 divided by the first resistor 106 and the second resistor 108 feeding voltage back to the comparator 102, where the comparison between this feedback voltage and a reference voltage vREFDC is taken place therein so as to control the gate of the NMOS power transistor. A steady first internal voltage VINT1 is thus generated thereof.

[0026] Referring to FIG. 4, a circuit block diagram of the second phase internal voltage generator 200 of the two phase internal voltage generator shown in FIG. 2 is illustrated therein. In FIG. 4, there is the two phase internal voltage generator according to one preferred embodiment of this present invention, wherein the second phase internal voltage generator 200 comprises a voltage pump generator 202, an input gate voltage generator 204, and a power output circuit 208. The voltage pump generator 202 pumps up and external voltage VEXT of the external voltage source to provide a pumped voltage VPP according to the first control voltage CHRDY1. The input gate voltage generator 204 steps down the pumped voltage VPP and regulates the voltage to input gate voltage vGI according to the second control signal CHRDY2. The power output circuit 206 provides a second internal voltage source VINT2 based on input gate voltage vGI where a NMOS power transistor 208 is introduced. As to the NMOS power transistor 208, the gate couples to the input gate voltage vGI, whereas a first source/drain terminal couples to the external voltage and a second source/drain terminal couples to the second internal voltage source.

[0027] It will be apparent to those skilled in the art that both the

foregoing NMOS power transistors 104 and 208 are not MOS type power transistors. Other larger power transistors that provide steadiness of voltage fall in the scope or spirit of the present invention.

[0028] In FIG. 5, an internal operation time chart of a two phase internal voltage generator in one preferred embodiment of the present invention is illustrated therein. Referring to FIG. 5 as well as FIG. 2 and FIG. 4, the internal operating steps of the two phase internal voltage generator in one preferred embodiment of this present invention are described as follows. The first-phase internal voltage generator 100 promptly provides a first internal voltage source upon an external voltage source being received, i.e. the external voltage VEXT being increased, so that the first internal voltage VINT1 increases accordingly. A first control signal CHRDY1 is actuated so as to activate voltage pump generator 202 to provided pumped voltage VPP. Thus a second control signal CHRDY2 is actuated by the pumped voltage VPP, so as to activate input gate voltage generator 204 to generate an input gate voltage vGI as well as to activate power output circuit 206 to steadily provide the second internal voltage source expressed as VINT2. Ultimately, a third control signal CHRDY3 is actuated for the

first phase internal voltage generator 200 to cut off the first internal voltage source therein.

[0029] Conclusively, according to ap23p23nother aspect of this present invention, a two phase internal voltage generating method is provided which conforms to an integrated circuit that is composed of a first phase internal voltage generator and a second phase internal voltage generator. Notice that the second phase internal voltage generator consumes relatively lower power than the first internal voltage generator, wherein the two phase internal voltage generating method comprises the following steps successively. An external voltage is firstly received, a first internal voltage source is provided promptly by the first phase internal voltage generator therein. The external voltage is pumped by the second phase internal voltage generator to obtain a pumped voltage that is stepped down and regulated in order to obtain an input gate voltage, whereas second internal voltage source is thus provided according to the input gate voltage therein. Ultimately the foregoing first phase internal voltage generator cuts off the first internal voltage source accordingly.

[0030] In this present invention a structure of two phase internal voltage generator is introduced. The first phase internal

voltage generator which is more power consuming promptly provides a steady first internal voltage source. As the second internal voltage provided by the second phase internal voltage generator is steadied, the first internal voltage generator cuts off the first internal voltage therein, so as to improve the issue over power consumption.

[0031] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.